

<b>Notice of References Cited</b>		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		10/646,658	LIANG, CHUNLIN	
		Examiner	Art Unit	Page 1 of 1
		Eric B. Chen	1765	

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,972,758	10-1999	Liang, Chunlin	438/294
	B	US-4,888,300	12-1989	Burton, Gregory N.	438/404
	C	US-6,268,637	07-2001	Gardner et al.	257/522
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Streetman, Solid State Electronic Devices, 1990, Prentice Hall, 3rd ed., pp. 300-301, 324.
	V	Wolf et al., Silicon Processing for the VLSI Era, 1986, Lattice Press, Vol. 1, pp. 280-281.
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.